REMARKS/ARGUMENTS

In this amendment, no claims are amended, canceled, or added. Thus, claims 1-22 remain pending.

Rejection under 35 USC §102(b) and 103(a), Rinaldi

Claims 1-2, 5-8, 11-12 and 15-22 were rejected under 35 U.S.C. 102(b) as being anticipate by Rinaldi et al (US Patent No. 6,327,002 Bl). Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rinaldi et al. Claims 3-4 and 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rinaldi et al in view of the admitted prior art (Figs. 1A & 1B, and page 2, [0005]-[0006]).

Claims 1-10, 17-19

Claim 1 is allowable as Rinaldi does not teach or suggest each and every element of claim 1. For example, claim 1 recites:

> *an encoder coupled to an output of the pixel pipeline circuit and configured to convert the pixel stream to digital sample values for a target analog signal representing the pixel stream in the target format, thereby generating a base data stream at a base sampling rate;*
>
> *a supersampling circuit coupled to an output of the encoder and configured to generate a supersampled data stream at a supersampling rate from the base data stream, the supersampling rate being higher than the base sampling rate.*

Rinaldi is directed to a graphics controller bypass path that skips processing by the graphics controller 24, e.g., when a received video signal does not need to be stored as frames and be encoded, thus reducing extra processing. *See Rinaldi*, col. 5 lines 13-16 and col. 1 lines 37-50. The relevant bypass path is from a video decoder 20 to an output module 21. *Id.*, Fig. 1. In the decoder 20, ADCs 58, 60 create digital sample values of the input analog signal. *Id.*, Fig. 2 and col. 3 lines 39-41. These sample values are simply a digital representation of the analog voltage values, and are not pixel values. The digital sample values are filtered by comb filter 52 and may be processed by modules 56 and 66 on their way to switching matrix 68. *Id.*, Fig. 2 and col. 3 lines 48-55. Rinaldi does not mention what type of processing is done by modules 56 and 66 or why it is done. The input switching matrix 68 selects signals to send to

upsampling circuit 70 based on whether processing on the digital samples was desired. *Id.*, col. 4 lines 2-6. Note that none of the above mentioned elements are coupled with pixel data in frame buffer 26. *Id.*, Fig. 1.

The Office Action asserts that the input switching matrix 68 converts "*the pixel stream to digital sample values for a target analog signal*," as recited by claim 1. However, the matrix 68 is simply multiplexors that determine whether processed or non-processed digital sample values are sent to the upsampling module 70. *Id.*, col. 3 lines 63-66. Thus, the matrix 68 does not convert input signals from one representation to another. Specifically, since its input is already represented as digital samples of the input analog signal, the matrix 68 cannot and does not convert its input to the same representation. Accordingly, Rinaldi does not teach or suggest "*an encoder ... [that converts] the pixel stream to digital sample values for a target analog signal,*" as recited in claim 1.

Moreover, since matrix 68 simply directs signals, it does not perform any sampling, and thus does not teach or suggest "*generating a base data stream at a base sampling rate,*" as recited in claim 1.

As matrix 68 does not create a base data stream at a base sampling rate, upsampling module 70 does not sample at a rate "*higher than the base sampling rate*," as recited in claim 1. Also, upsampling module 70 matches the sampling frequency to the desired output sampling frequency, and thus does not take it higher than that of a target analog signal.

For at least these reasons, claim 1 is allowable over Rinaldi. As claim 1 is allowable, dependent claims 2-10 are also allowable for at least the same rationale.

Applicants submit that independent claim 17, and its dependent claims 18-19, are allowable for at least the same reasons as claim 1.

Claims 11-16, 20-22

Claim 11 is allowable as Rinaldi does not teach or suggest each and every element of claim 11. For example, claim 11 recites:

> *a supersampling circuit coupled to an output of the pixel pipeline circuit and configured to generate a supersampled pixel stream comprising a second*

number of digital pixel values per line, the second number being greater than the first number, at a supersampling rate higher than the base pixel rate;

an encoder coupled to an output of the supersampling circuit and configured to convert the supersampled pixel stream to digital sample values for a target analog signal representing the supersampled pixel stream in the target format, thereby generating a supersampled data stream at an enhanced sampling rate.

As described above, upsampling circuit 70 receives digital samples of an analog signal, and not a pixel stream. Thus, Rinaldi does not teach or suggest a supersampling circuit "*to generate a supersampled pixel stream*," as recited in claim 11.

Additionally, the output switching matrix 72 does not perform any functionality different than the input switching matrix 68. *Id.*, col. 4 lines 8-11. Thus for at least the same reasons stated for claim 1, matrix 72 does not correspond to an encoder that converts a "*supersampled pixel stream to digital sample values for a target analog signal*," as recited in claim 1. Accordingly, Rinaldi does not teach or suggest this limitation.

For at least these reasons, claim 11 is allowable over Rinaldi. As claim 11 is allowable, dependent claims 12-16 are also allowable for at least the same rationale.

Applicants submit that independent claim 20, and its dependent claims 21-22, are allowable for at least the same reasons as claim 11.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

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